

<b>PTO-1449 REPRODUCED</b>  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>October 27, 2003</b>  (Use several sheets if necessary)	<b>ATTORNEY DOCKET NO.</b> 2789.2003-001		<b>DIV. OF APPLICATION NO.</b> 09/557,564	
	<b>APPLICANT</b> William J. Dally, <i>et al.</i>			
	<b>FILING DATE</b>		<b>CONFIRMATION NO.</b>	<b>GROUP</b> 2609

U.S. PATENT DOCUMENTS				
EXAM- INER INI- TIAL	REF. NO.	DOCUMENT NUMBER	ISSUE DATE / PUBLICATION DATE	NAME
/EO/	AA	6,114,915	09-2000	Huang et al.
/EO/	AB	5,361,254	11-1994	Storck et al.
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<b>EXAMINER</b> /Eunsook Choi/	<b>DATE CONSIDERED</b> 07/06/2007
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
/EC/	AR	Dally, William J. and Poulton, John W., <i>Digital Systems Engineering</i> , Cambridge University Press, 1998, pp. 428-447, 537-540 and 547-548.
/EC/	AS	Kim, Weigant and Gray, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design," ISCAS, 1994, pp. 31-34.
/EC/	AT	Waizman, A., "A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," IEEE International Solid-State Circuits Conference, 1994, pp. 298-299.
/EC/	AU	Dally, William J. and Poulton, John W., "Transmitter Equalization for 4Gb/s Signaling," IEEE Micro, Jan-Feb 1997, pp. 48-56.
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